

### **In the Specification**

At page 1 before the "Technical Field" section, please insert the following:

#### **RELATED PATENT DATA**

This patent is a divisional application of U.S. Patent Application Serial No. 10/300,175, filed November 19, 2002, entitled "Method of Isolating a SRAM Cell", naming Michael P. Violette as inventor; which is a divisional of U.S. Patent Application Serial No. 09/565,429, filed May 5, 2000, entitled "A Method of Isolating a SRAM Cell", naming Michael P. Violette as inventor; which is a continuation of U.S. Patent Application Serial No. 08/960,875, now U.S. Patent No. 6,103,579, filed October 30, 1997, entitled "A Method of Isolating a SRAM Cell", naming Michael P. Violette as inventor; which is a continuation of U.S. Patent Application Serial No. 08/819,546, filed March 17, 1997, now abandoned; which is a continuation of U.S. Patent Application Serial No. 08/594,747, filed January 31, 1996, now abandoned, the disclosures of which are incorporated by reference.

Please amend the paragraph beginning on page 4, lines 9 through 20, as follows:

A memory flip-flop such as that described typically forms one memory element of an integrated array of static memory elements. A plurality of access transistors, such as access transistors 30 and 32, are used to selectively address and access individual memory elements within the array. Access transistor 30 has one active terminal 58 connected to cross-coupled inverter output 20. Access transistor 32 has one active terminal 60 connected to cross-coupled inverter output 22. A pair of complementary column or bit lines 34 and 36 ~~shown~~, are connected to the remaining active terminals 56 and 54 of access transistors 30 and 32, respectively. A row or word line 38 is connected to the gates of access transistors 30 and 32. In the illustrated embodiment, access transistors 30 and 32 are n-channel transistors.

Please amend the paragraph beginning on page 7, line 11 through page 8, line 15, as follows:

The invention provides a static random access memory cell comprising a first p-channel pullup transistor having a gate, drain, and source; a first n-channel pulldown transistor having a gate, drain, and source; a second p-channel pullup transistor having a gate, drain, and source; a second n-channel pulldown transistor having a gate, drain, and source; the source of the first pullup transistor being adapted to be connected to a first voltage;

the source of the second pullup transistor being adapted to be connected to the first voltage; the drain of the first pulldown transistor being connected to the drain of the first pullup transistor; the drain of the second pulldown transistor being connected to the drain of the second pullup transistor; the source of the first pulldown transistor being adapted to be connected to a second voltage lower than the first voltage; the source of the second pulldown transistor being adapted to be connected to the second voltage; the gate of the first pullup transistor being connected to the gate of the first pulldown transistor; the gate of the second pullup transistor being connected to the gate of the second pulldown transistor; the first pullup transistor and the first pulldown transistor together defining a first ~~inverter~~ inverter having an output defined by the drain of the first pulldown transistor and an input defined by the gate of the first pulldown transistor, the second pullup transistor and the second pulldown transistor together defining a second ~~inverter~~ inverter having an output defined by the drain of the second pulldown transistor and an input defined by the gate of the second pulldown transistor, the input of the first ~~inverter~~ inverter being connected to the output of the second ~~inverter~~ inverter, and the input of the second ~~inverter~~ inverter being connected to the output of the first ~~inverter~~ inverter; and a p-channel isolation transistor connected between the drain of the first pullup transistor and the drain of the second pullup transistor, and having a gate.

Please amend the paragraph beginning on page 8, line 16 through page 9, line 3, as follows:

In one aspect of the invention, a static random access memory cell comprises a first ~~inverter~~ inverter including a first p-channel pullup transistor, and a first n-channel pulldown transistor in series with the first p-channel pullup transistor; a second ~~inverter~~ inverter including a second p-channel pullup transistor, and a second n-channel pulldown transistor in series with the second n-channel pullup transistor, the first ~~inverter~~ inverter being cross-coupled with the second ~~inverter~~ inverter, the first and second pullup transistors sharing a common active area; a first access transistor having an active terminal connected to the first ~~inverter~~ inverter; a second access transistor having an active terminal connected to the second ~~inverter~~ inverter; and an isolator isolating the first pullup transistor from the second pullup transistor.

Please amend the paragraph beginning on page 9, lines 4 through 18, as follows:

In one aspect of the invention, a method of manufacturing a static random access memory cell including first and second cross-coupled ~~inverters~~ inverters, each ~~inverter~~ inverter including a p-channel transistor connected in series with an n-channel transistor, the p-channel transistors having sources that are connected to each other and that are adapted to be connected to a common first voltage, and the p-channel transistors having

respective drains; the n-channel transistors having respective sources that are connected to each other and that are adapted to be connected to a common second voltage, lower than the first voltage, and the n-channel transistors having respective drains; the method comprising the following steps: providing a silicon substrate; defining the first and second ~~inverters~~ inverters relative to the substrate and including an active area common to drains of the p-channel transistors; and defining an isolation gate relative to the common active area, between the drains of the p-channel ~~transistor~~ transistors.

Please amend the paragraph beginning on page 9, line 19 through page 10, line 12, as follows:

In one aspect of the invention, a method of manufacturing a wafer including a plurality of static random access memory cells, each cell including first and second cross-coupled ~~inverters~~ inverters, each ~~inverter~~ inverter including a p-channel transistor connected in series with an n-channel transistor, the p-channel transistors having sources that are connected together and that are adapted to be connected to a common first voltage, and having respective drains; the n-channel transistors having sources that are connected together and that are adapted to be connected to a common second voltage, lower than the first voltage, and having respective drains; the method comprising the following steps: providing a silicon substrate; defining active areas relative to the substrate for the static

random access memory cells, the active areas including an active area having the general shape of a stepladder, including two parallel, spaced apart sides, and a plurality of parallel, spaced apart portions extending between the sides, such that the sides define drains of a plurality of the p-channel transistors; and defining respective isolation gates relative to active areas, between the drains of the p-channel transistors within each static random access memory cell.

Please amend the paragraph beginning on page 13, lines 3 through 14, as follows:

The desired shape of the H-shaped regions 42 is indicated in FIG. 4 by outer dashed line 88. This is the shape of the active area as drawn on a reticle employed in defining the H-shaped regions 42. Inner dashed line 90 represents the shape of the area after photolithography (I-line 365 nm). Finally, the shape after aggressive LOCOS isolation (described above in the Background of the Invention) is illustrated with solid line 92. Encroachment takes place along two dimensions; i.e., along both the length and the width of the "H". The most extreme pullback occurs at the ends of the legs of the "H" where the drains 70 and 72 of the p-channel transistors P1 and P2 are defined. Also, the polysilicon has an associated spacer (e.g., 800 angstroms wide) which reduces the size of the active area ~~over~~ even further.

Please amend the paragraph beginning on page 14, line 23 through page 15, line 15, as follows:

The inventor of the present invention has accomplished the necessary isolation by providing an isolator which isolates the pullup transistor P1 from the pullup transistor P2. More particularly, the isolator comprises an isolation gate 84 defined relative to the common active area, between the drains 70 and 72 of the p-channel transistors P1 and P2. In the illustrated embodiment, polysilicon is employed to define the isolation gate 84. By causing polysilicon 44 to intersect the common active area, an isolation p-channel transistor 82 is defined (FIG. 5) between the ~~gate~~ drains 70 and 72. Similarly, an isolation p-channel transistor 83 is defined for an adjacent memory cell.

Please amend the paragraph beginning on page 15, lines 8 through 15, as follows:

The isolation gate is adapted to be connected to a voltage higher than Vss. More particularly, the isolation gate is adapted to be connected to a voltage sufficient to turn off (tri-state) the isolation transistor, and thus isolate ~~gate drain~~ drain 70 from ~~gate drain~~ drain 72 (except for leakage current). In one embodiment, the isolation gate 84 is connected to the sources of the p-channel transistors P1 and P2. More particularly, in the illustrated embodiment, the isolation gate 84 is connected to the Vcc metal.

Please amend the paragraph beginning on page 15, line 16 through page 16, line 3, as follows:

Other than the common active area shared by drains 70 and 72, and the isolation gate 84, the embodiment shown in FIGS. 5-7 is substantially identical to the embodiment shown in FIGS. 2-3, like reference numerals indicating like components. The silicon processing steps employed in forming the embodiment shown in FIG. 6 is ~~substantial~~ substantially identical to the silicon processing steps employed in manufacturing the embodiment shown in FIG. 2, except for the formation of the common active area (the ladder shaped active areas of FIG. 7 are formed at the same stage in the process, and in a similar manner, as the H-shaped active areas of FIG. 2). FIG. 5 also shows a parasitic transistor 40 formed because of an intersection of polysilicon with an active area, which is not shown in FIG. 1.

Please amend the paragraph beginning on page 16, lines 4 through 11, as follows:

Thus, a layout for manufacturing static random access memory cells has been provided which results in reduced size of each cell. Each cell includes first and second cross-coupled ~~inverters~~ inverters, each ~~inverter~~ inverter including a first p-channel pullup transistor, and a first n-channel pulldown transistor in series with the first p-channel pullup transistor; the first and second pullup transistors sharing a common active area; and an isolator isolating the first pullup transistor from the second pullup transistor.